EXHIBIT 5

"Claims as filed in
U.S. Application No. 10/801,308"

CLAIMS:

1. A method, comprising:

monitoring processor tasks and associated processor loads therefor that are allocated to be performed by respective sub-processing units associated with a main processing unit;

re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and

commanding the sub-processing units that are not scheduled to perform any tasks into a low power consumption state.

2. The method of claim 1, wherein:

each of the sub-processing units include at least one of: (i) a power supply interrupt circuit; and (ii) a clock interrupt circuit; and

the method includes using at least one of the power supply interrupt circuit and the clock interrupt circuit to place the sub-processing units into the low power consumption state includes in response to the power-off command.

3. The method of claim 2, wherein each of the sub-processing units includes a power supply and the power supply interrupt circuit; and

the method includes using the power supply interrupt circuit to shut down the power supply in response to the power-off command to place the given sub-processing unit into the low power consumption state.

4. The method of claim 1, wherein:

the main processing unit includes a task load table containing the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and

the method includes using the main processing unit to update the task load table in response to any changes in tasks and loads.

5. The method of claim 4, wherein:

the main processing unit includes a task allocation unit operatively coupled to the task load table; and

the method includes using the main processing unit to re-allocate at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks.

6. The method of claim 5, further comprising re-allocating all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

7. The method of claim 5, further comprising re-allocating some of the tasks of a given one of the sub-processing units to one or more of the other sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

8. The method of claim 1, further comprising reducing the dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable clock frequency control.

9. The method of claim 1, further comprising reducing the static and dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable power supply (Vdd) control.

10. An apparatus, comprising:

a plurality of sub-processing units, each operable to perform processor tasks; and

a main processing unit operable to: (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; (ii) re-allocate at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and (iii) issue a power-off command indicating that the sub-processing units that are not scheduled to perform any tasks should enter a low power consumption state.

11. The apparatus of claim 10, wherein the sub-processing units include at least one of: (i) a power supply interrupt circuit; and (ii) a clock interrupt circuit, each of which are operable to place the given sub-processing unit into the low power consumption state in response to the power-off command.

12. The apparatus of claim 11, wherein each of the sub-processing units includes a power supply and the power supply interrupt circuit, and the power supply interrupt circuit is operable to shut down the power supply in response to the power-off command to place the given sub-processing unit into the low power consumption state.

13. The apparatus of claim 10, wherein:

the main processing unit includes a task load table containing the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and

the main processing unit is operable to update the task load table in response to any changes in tasks and loads.

14. The apparatus of claim 13, wherein: the main processing unit includes a task allocation unit operatively coupled to the task load table and operable to re-allocate at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks.

15. The apparatus of claim 14, wherein the task allocation unit is operable to re-allocate all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

16. The apparatus of claim 15, wherein the main processing unit includes a power supply controller

operatively coupled to the task allocation unit and operable to issue the power-off command signal to the given one of the sub-processing units in response to an indication from the task allocation unit that the given one of the sub-processing units is not scheduled to perform any tasks.

17. The apparatus of claim 14, wherein the task allocation unit is operable to re-allocate some of the tasks of a given one of the sub-processing units to one or more of the other sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

18. The apparatus of claim 15, wherein the main processing unit includes a power supply controller operatively coupled to the task allocation unit and operable to issue the power-off command signal to the given one of the sub-processing units in response to an indication from the task allocation unit that the given one of the sub-processing units is not scheduled to perform any tasks.

19. The apparatus of claim 10, wherein at least one of the main processing unit and one or more of the sub-processing units are operable to carry out variable clock frequency control in order to reduce the dynamic power dissipation of at least one of the sub-processing units.

20. The apparatus of claim 10, wherein at least one of the main processing unit and one or more of the sub-processing units are operable to carry out variable power supply (Vdd) control in order to reduce the static and

dynamic power dissipation of at least one of the sub-processing units.

21. The apparatus of claim 10, wherein at least one of the main processing unit and one or more of the sub-processing units are formed using a silicon-on-insulator fabrication process.

22. The apparatus of claim 10, wherein the main processing unit is at least one of remotely located from or locally located with one or more of the sub-processing units.

23. The apparatus of claim 10, wherein one or more of the sub-processing units are remotely located from one another.

24. The apparatus of claim 10, wherein the sub-processing units employ substantially heterogeneous computer architectures or a homogeneous computer architecture.

25. A main processor operating under the control of a software program to perform steps, comprising:

monitoring processor tasks and associated processor loads therefor that are allocated to be performed by respective sub-processing units associated with the main processing unit;

re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and

commanding the sub-processing units that are not scheduled to perform any tasks into a low power consumption state.

26. The processor of claim 25, wherein:

each of the sub-processing units include at least one of: (i) a power supply interrupt circuit; and (ii) a clock interrupt circuit; and

at least one of the power supply interrupt circuit and the clock interrupt circuit respond to the power-off command by placing the sub-processing units into the low power consumption state.

27. The processor of claim 26, wherein each of the sub-processing units includes a power supply and the power supply interrupt circuit; and

the power supply interrupt circuit responds to the power-off command by shutting down the power supply to place the given sub-processing unit into the low power consumption state.

28. The processor of claim 25, wherein:

the main processing unit includes a task load table containing the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and

the steps include updating the task load table in response to any changes in tasks and loads.

29. The processor of claim 28, wherein:

the main processing unit includes a task allocation unit operatively coupled to the task load table; and

the steps include re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks.

30. The processor of claim 29, further comprising re-allocating all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

31. The processor of claim 29, further comprising re-allocating some of the tasks of a given one of the sub-processing units to one or more of the other sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

32. The processor of claim 25, further comprising reducing the dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable clock frequency control.

33. The processor of claim 25, further comprising reducing the static and dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable power supply (Vdd) control.

34. An apparatus, comprising:

a plurality of sub-processing units, each operable to perform processor tasks; and

a bus circularly interconnecting the sub-processing units such that transfers between any two sub-processing units may occur directly as between adjacent sub-processing units or through one or more intermediate sub-processing units as between more distant sub-processing units,

wherein the sub-processing units are operable to: (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; (ii) re-allocate at least some of the tasks based on their associated processor loads.

35. The apparatus of claim 34 wherein the sub-processing units are arranged in groups and the re-allocation of one or more tasks of a sub-processing unit within a given one of the groups maintains such tasks within the given group.

36. The apparatus of claim 34 wherein the re-allocation of the tasks is performed such that at least one of the sub-processing units is not scheduled to perform any tasks.

37. The apparatus of claim 36, wherein the sub-processing units that are not scheduled to perform any tasks are operable to enter a low power consumption state.

38. The apparatus of claim 34, wherein:

the sub-processing units are operable to access a task load table containing the processor tasks and associated

processor loads therefor that are allocated to be performed by the respective sub-processing units; and

the sub-processing units are operable to update the task load table in response to any changes in tasks and loads.

39. The apparatus of claim 38, wherein the sub-processing units are operable to re-allocate all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.